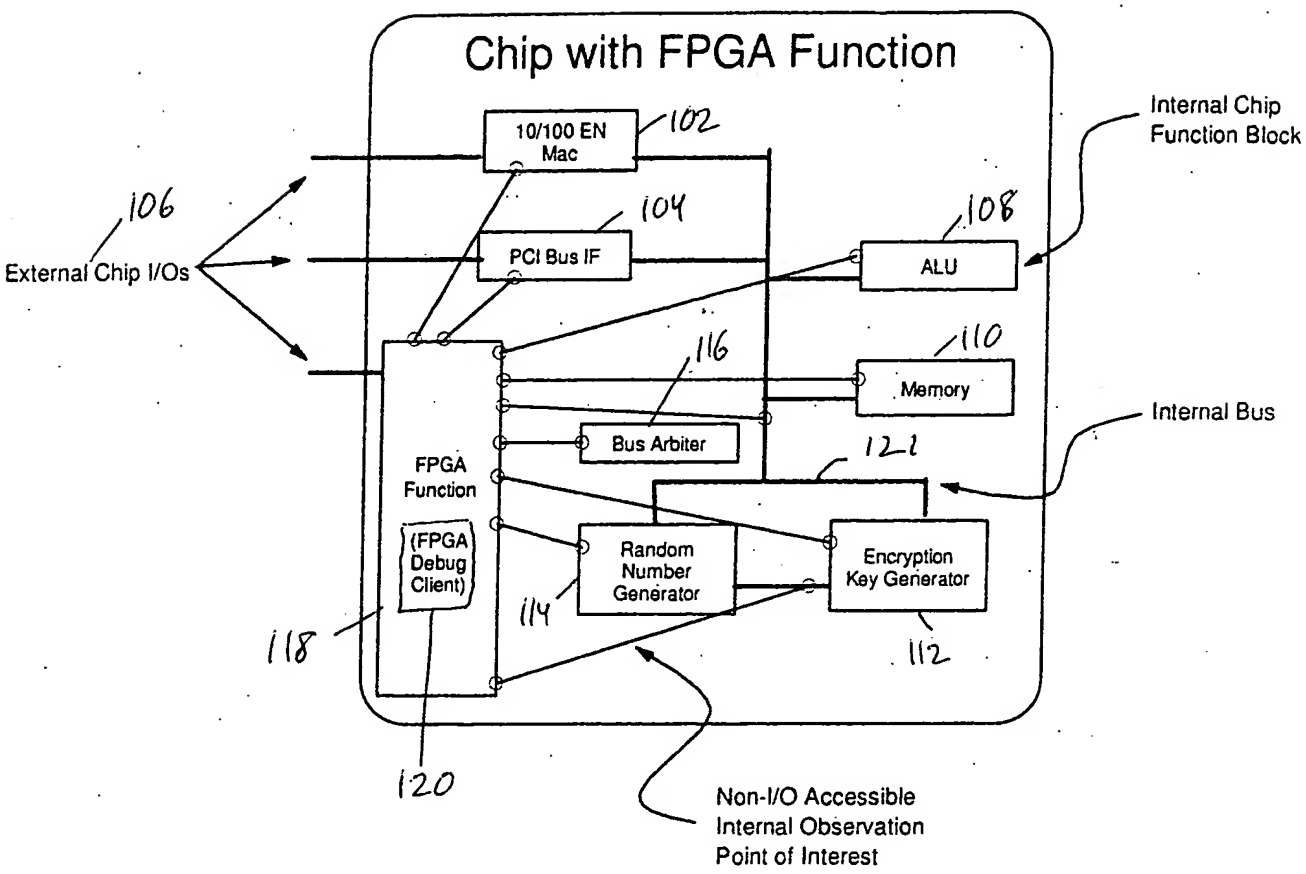
Chip with FPGA Function
10/100 EN Mac
102
PCI Bus IF
104
106
External Chip I/Os
ALU
108
Internal Chip Function Block
Memory
110
116
Bus Arbiter
Internal Bus
121
FPGA Function
(FPGA Debug Client)
Random Number Generator
114
Encryption Key Generator
112
118
120
Non-I/O Accessible Internal Observation Point of Interest
100

Fig. 1

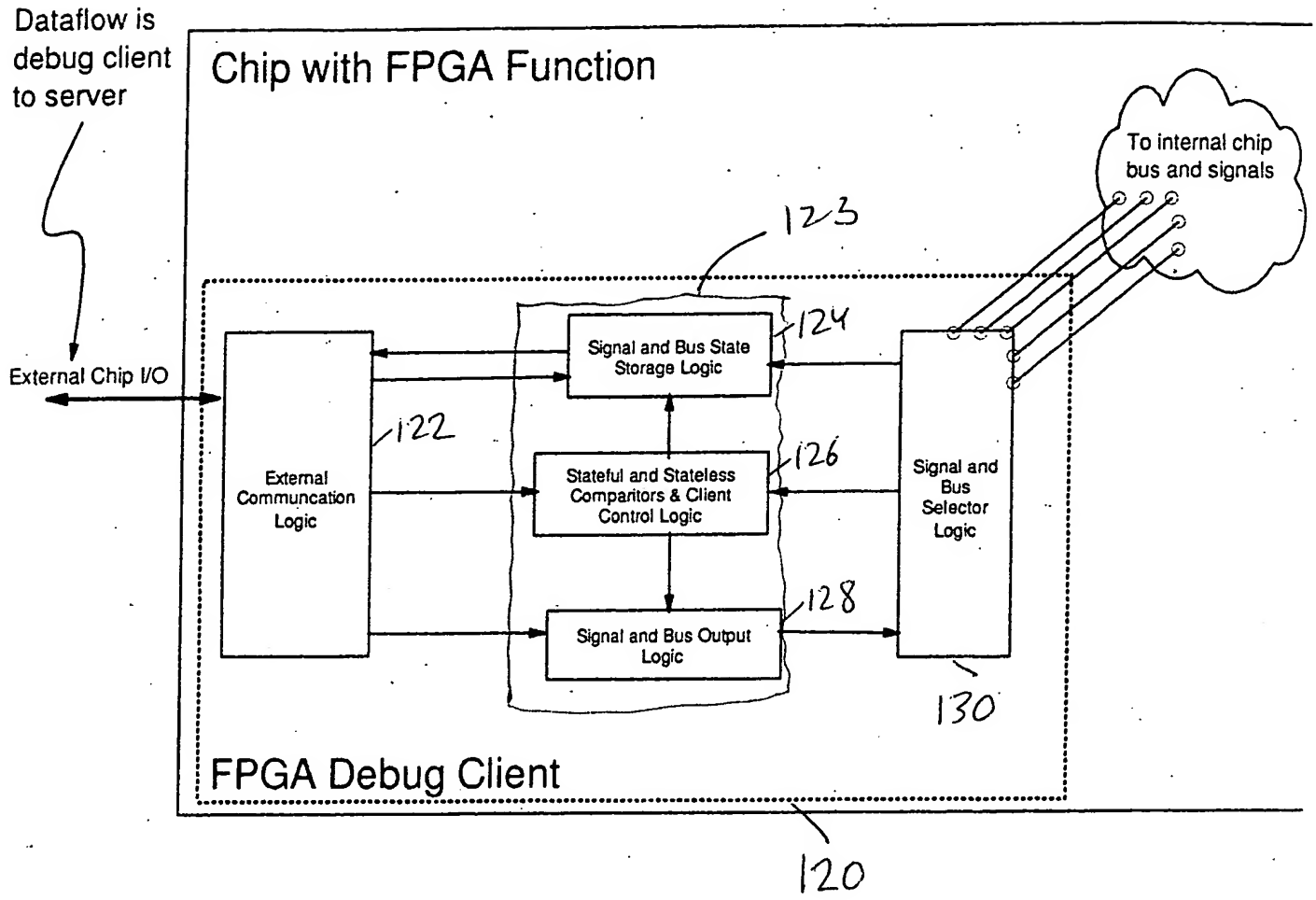
Dataflow is debug client to server
Chip with FPGA Function
To internal chip bus and signals
123
External Chip I/O
Signal and Bus State Storage Logic
124
122
External Communcation Logic
Stateful and Stateless Comparitors & Client Control Logic
126
Signal and Bus Selector Logic
128
Signal and Bus Output Logic
130
FPGA Debug Client
120

Fig. 2

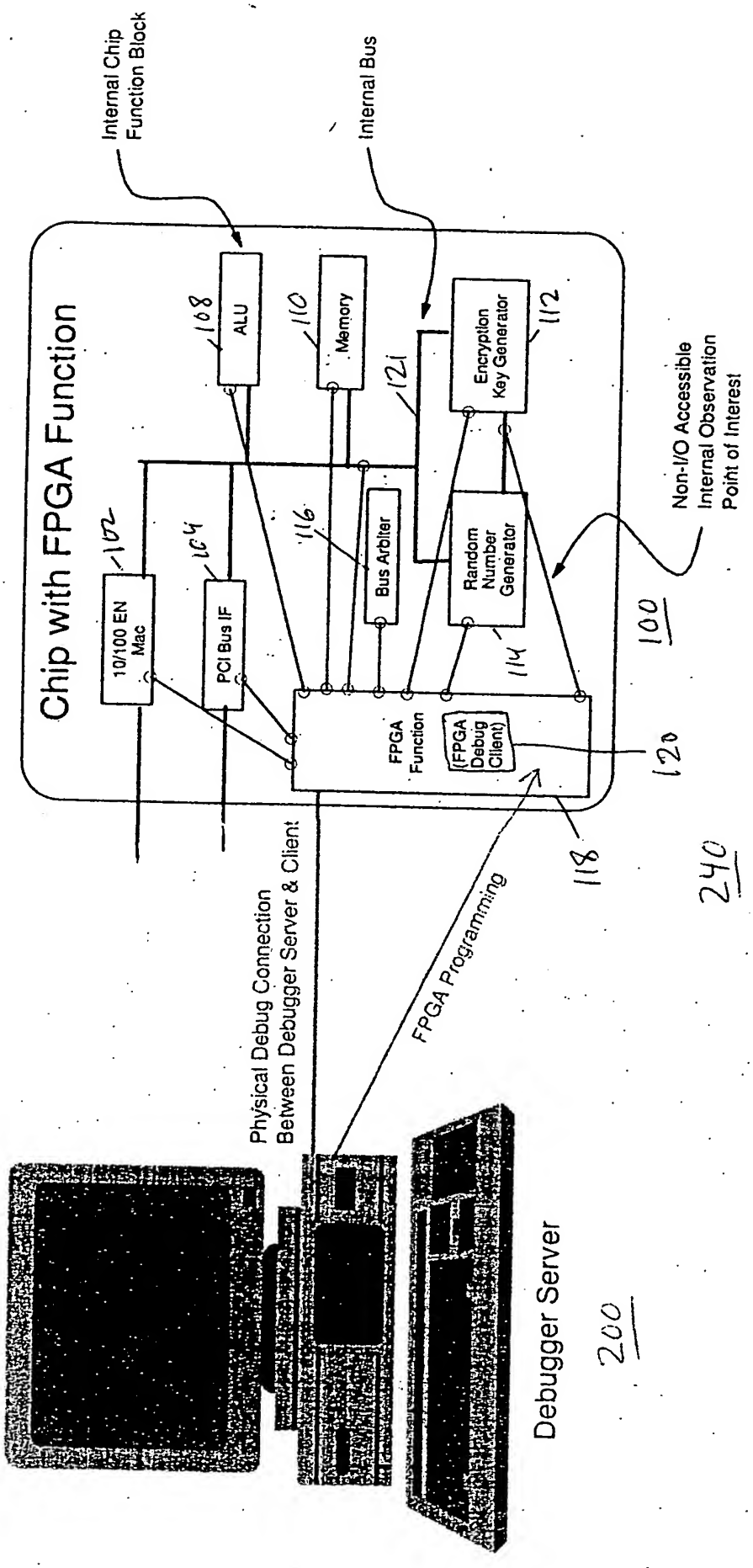

Fig. 3